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MS-7418 (MS-6496)

Version 3.0

CPU:

Intel Dimondville

System Chipset:

Intel 945GC (North Bridge)

Intel ICH7(South Bridge)

On Board Chipset:

BIOS -- SPI

HD AUDIO CODEC(ALC888)

LAN -- Realtek RTL8111C

Clock Generator - ICS954119

Main Memory:

DDR II SO-DIMM x 1 (Max 2GB)

CF Card Connector for flash Memory

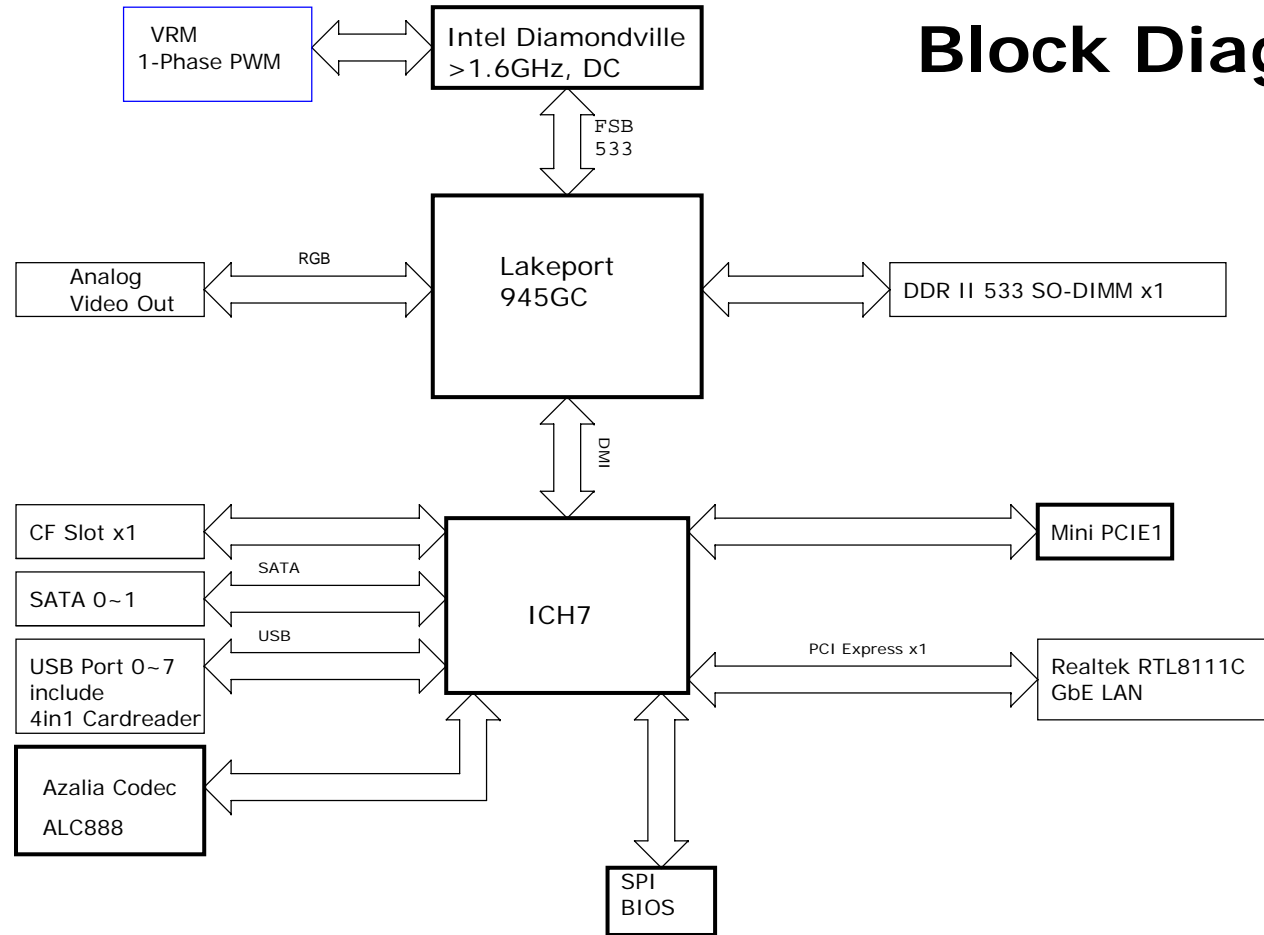
Expansion Slots:

Internal Mini PCIE x1

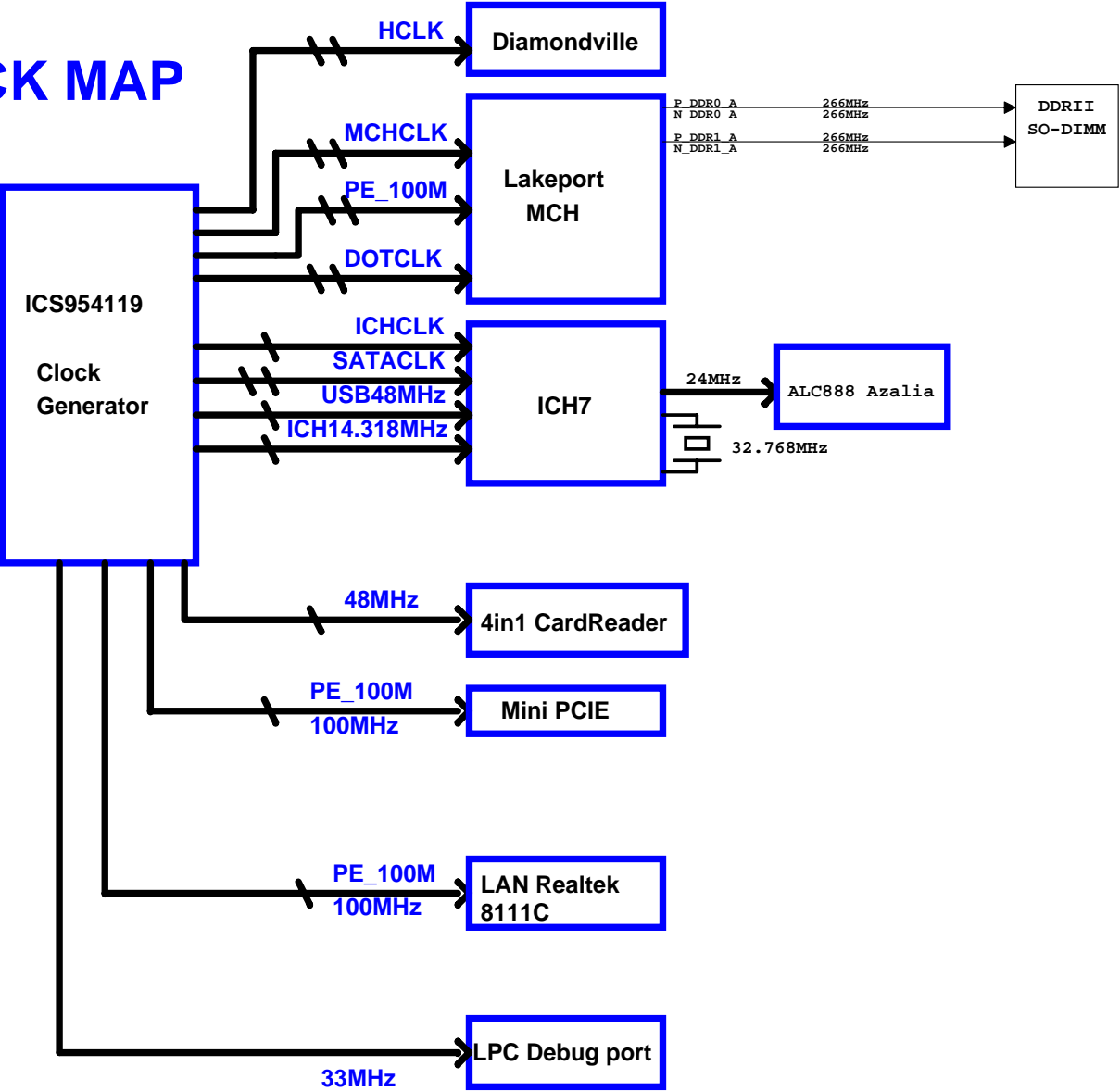
Intersil PWM:

Controller: 6314

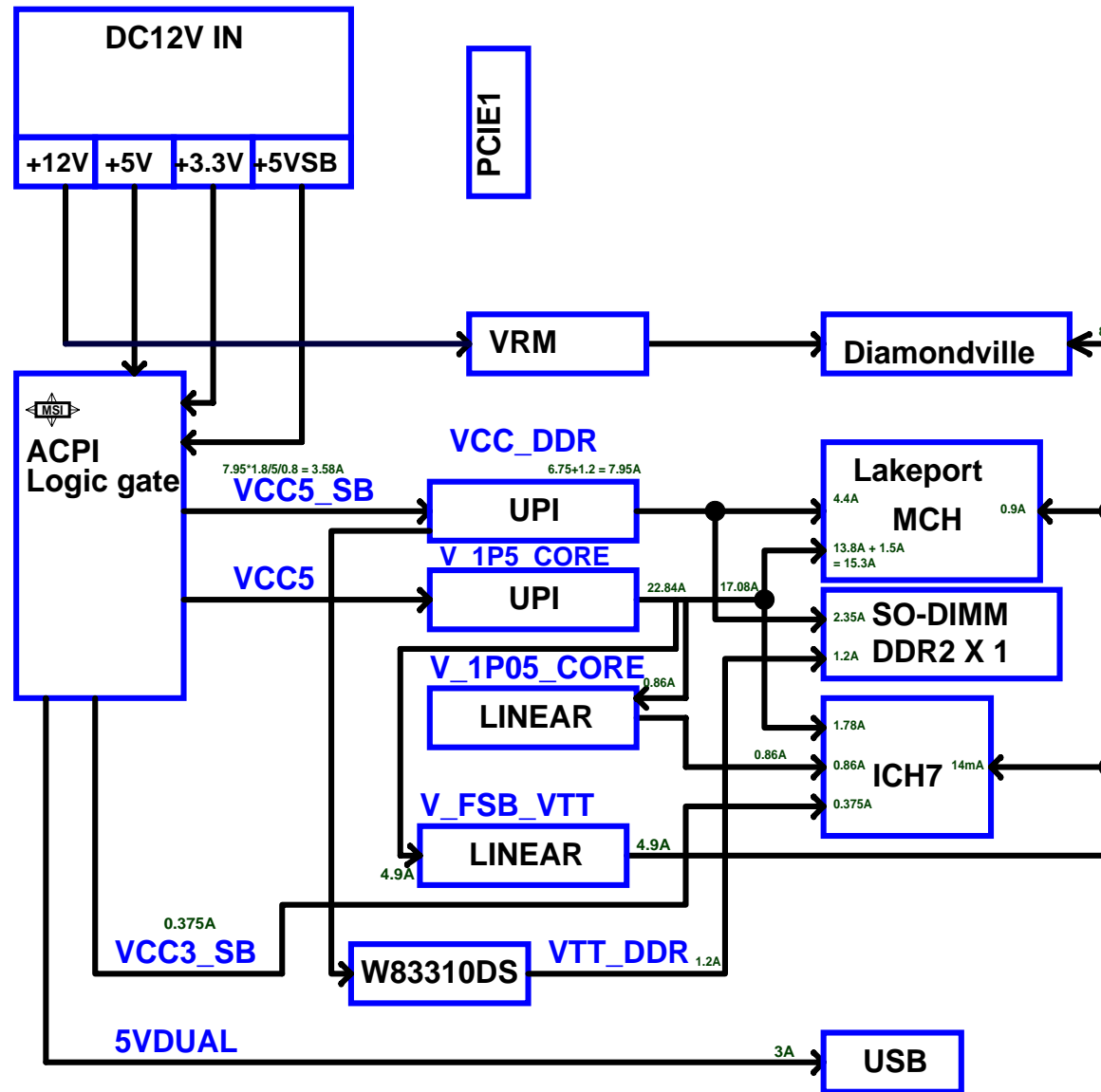
Block Diagram



CLOCK MAP



POWER MAP



ICH7

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name or status
GPIO[0]	SIO_SMI#	AB18	I/O	Vcc3p3	N	Y	5	Input	pull high VCC3
GPIO[1]	PCIREQ[5]#	C8	I/O	V5REF	N	Y	5	Input	PREQ#5
GPIO[2]	PIRQE#	G8	I/OD	V5REF	N	Y	5	Input	PIRQ#E
GPIO[3]	PIRQF#	F7	I/OD	V5REF	N	Y	5	Input	PIRQ#F
GPIO[4]	PIRQG#	F8	I/OD	V5REF	N	Y	5	Input	PIRQ#G
GPIO[5]	PIRQH#	G7	I/OD	V5REF	N	Y	5	Input	PIRQ#H
GPIO[6]	ATADET0	AC21	I/O	Vcc3p3	N	Y	3.3	Input	ATADET0
GPIO[7]	GPI7	AC18	I/O	Vcc3p3	N	Y	3.3	Input	pull high VCC3
GPIO[8]	SIO_PME#	E21	I/O	VccSus3p3	N	Y	3.3	Input	SIO_PME# pull high VCC3_SB
GPIO[9]	WLAN_PWRON	E20	I/O	VccSus3p3	N	Y	3.3	Output	pull high VCC3_SB
GPIO[10]	unmuxed	A20	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[11]	SMBALERT#	B23	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[12]	unmuxed	F19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[13]	unmuxed	E19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[14]	ADT7467_ALERT	R4	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[15]	unmuxed	E22	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[16]	unmuxed	AC22	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[17]	PCIGNT[5]#	D8	I/O	Vcc3p3	N	N	3.3	N/A	NC
GPIO[18]	unmuxed	AC20	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[19]	SATA1GP	AH18	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[20]	unmuxed	AF21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[21]	SATA0GP	AF19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[22]	PCIREQ[4]#	A13	I/O	Vcc3p3	N	N	3.3	Input	PREQ#4
GPIO[23]	LDRQ1#	AA5	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[24]	unmuxed	R3	I/O	VccSus3p3	N	N	3.3	No Change	NC
GPIO[25]	S1_3_LED	D20	I/O	VccSus3p3	Y	N	3.3	1	pull high VCC3_SB
GPIO[26]	unmuxed	A21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	unmuxed	B21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	unmuxed	E23	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC#2	C3	I/O	VccSus3p3	N	N	3.3	Input	OC#5
GPIO[30]	OC#2	A2	I/O	VccSus3p3	N	N	3.3	Input	OC#6
GPIO[31]	OC#2	B3	I/O	VccSus3p3	N	N	3.3	Input	OC#7
GPIO[32]	CLEAR_CMOS#	AG18	I/O	Vcc3p3	N	N	3.3	1	CLEAR_CMOS#, ONLY pull high VCC3
GPIO[33]	unmuxed	AC19	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[34]	unmuxed	U2	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[35]	unmuxed	AD21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[36]	SATA2GP	AH19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[37]	SATA3GP	AE19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[38]	unmuxed	AD20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[39]	unmuxed	AE20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[48]	GNT4#	A14	I/O	Vcc3p3	N	N	3.3	N/A	GNT4#
GPIO[49]	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	CPU	N/A	H_PWRGD
GPI[15..0] can configured to cause a SMI# or SCI.									

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39;36;23;21;19;7;0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31;29;15;8]: default as inputs and should be pulled up to VccSus3_3 if unused.

FWH Note: FWH GPs should only be used for static options, do not put dynamic nets on these				
GPIO	Pin#	Power	Tol	Signal Name
FPGI[0]	6	Main	3.3	pull-down
FPGI[1]	5	Main	3.3	pull-down
FPGI[2]	4	Main	3.3	pull-down
FPGI[3]	3	Main	3.3	pull-down
FPGI[4]	30	Main	3.3	pull-down

SIGNAL	DEVICE
MiniPCleRST#	MINI PCIE SLOT
TPMRST#	TPM
LANRST#	LAN 8111C
PCIRST_ICH7#	BUFFER IC
CF_RST#	CF_CARD
H_CPURST#	CPU
FWHRST#	LPT Debug port
MCHRST#	MCH

SMBCLK, SMBDATA, DDR2, PCIEX1, CLKGEN, ICH7, ADT7464

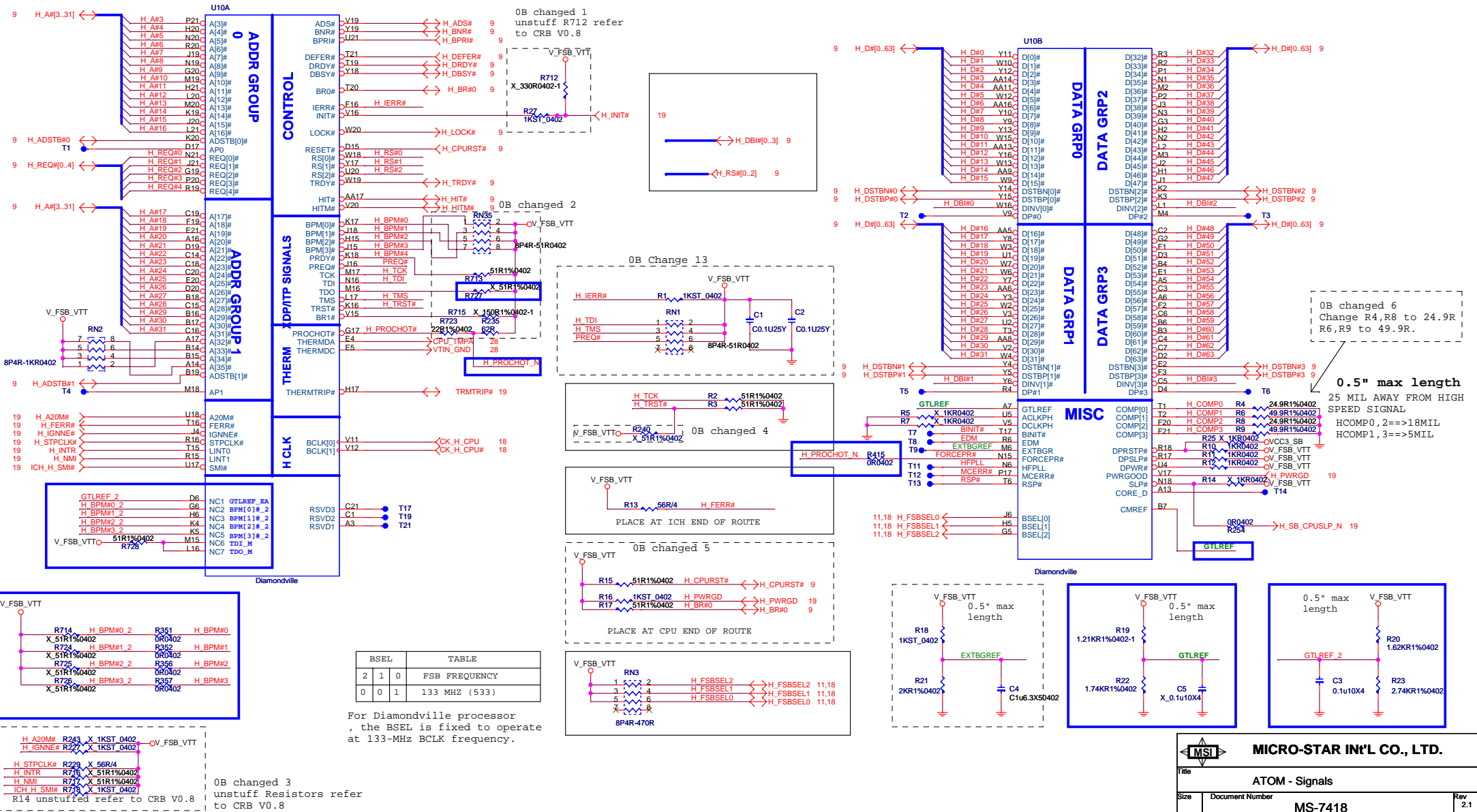
DDRII DIMM Config.

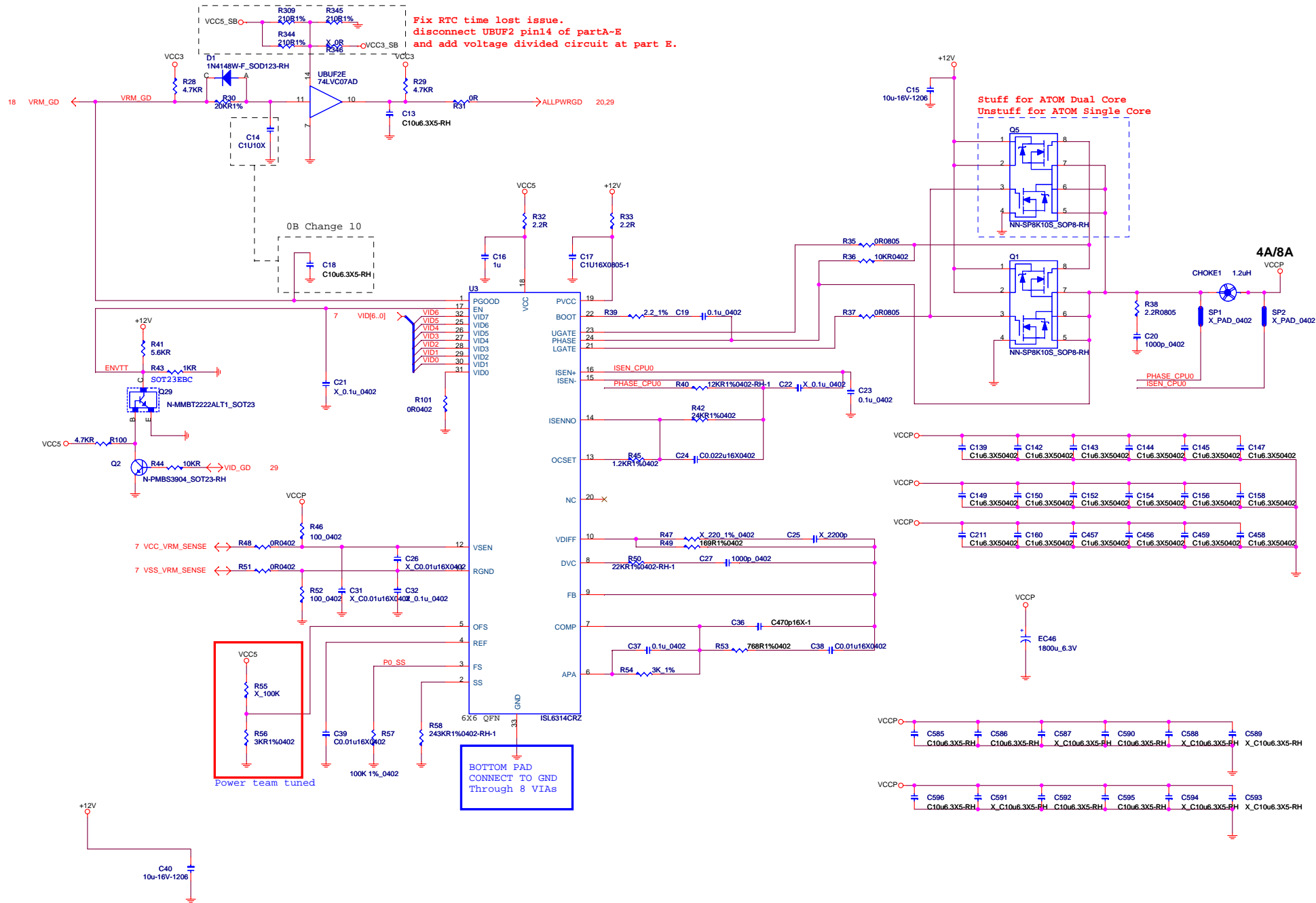
DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2

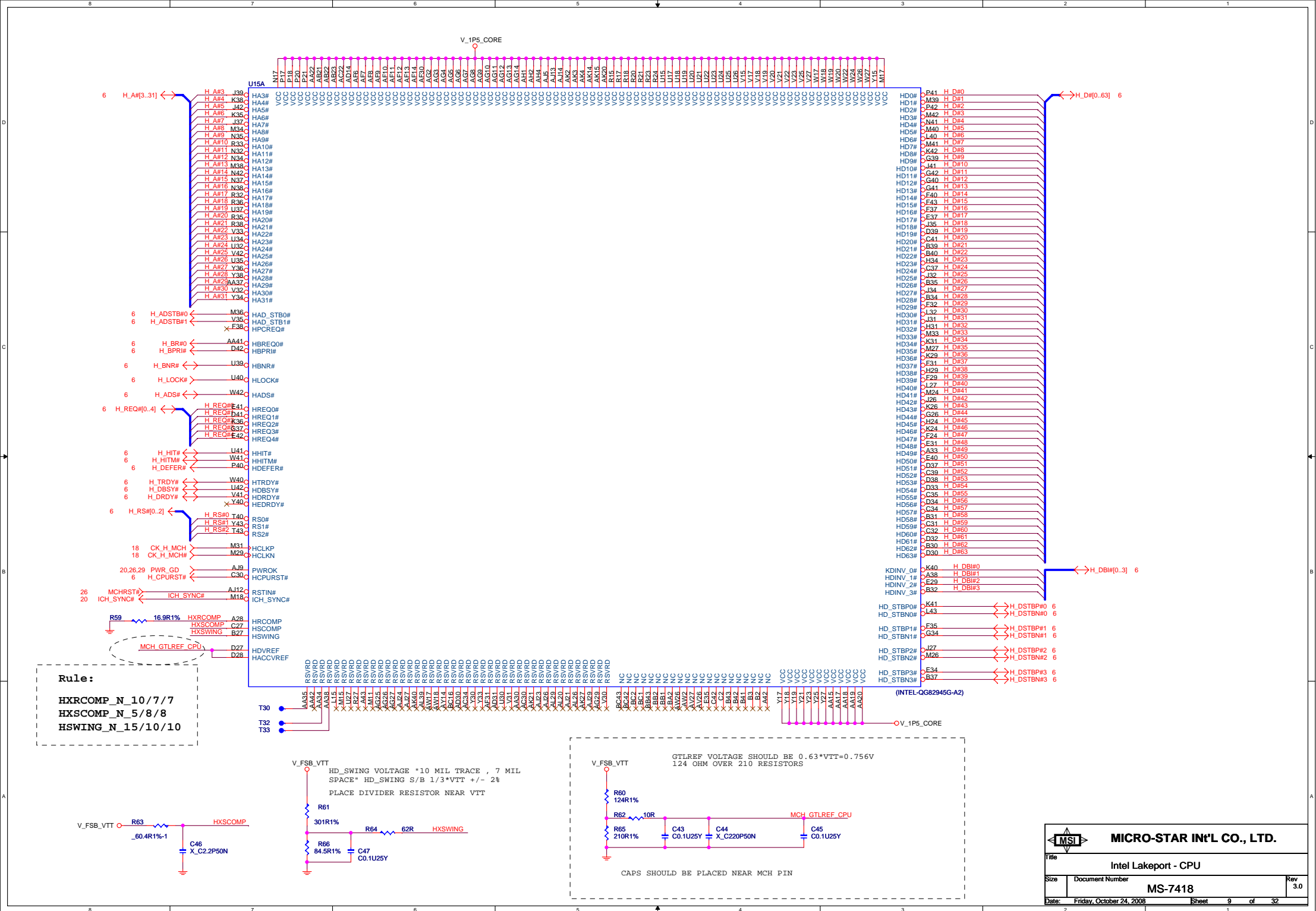
JUMPER SETTING

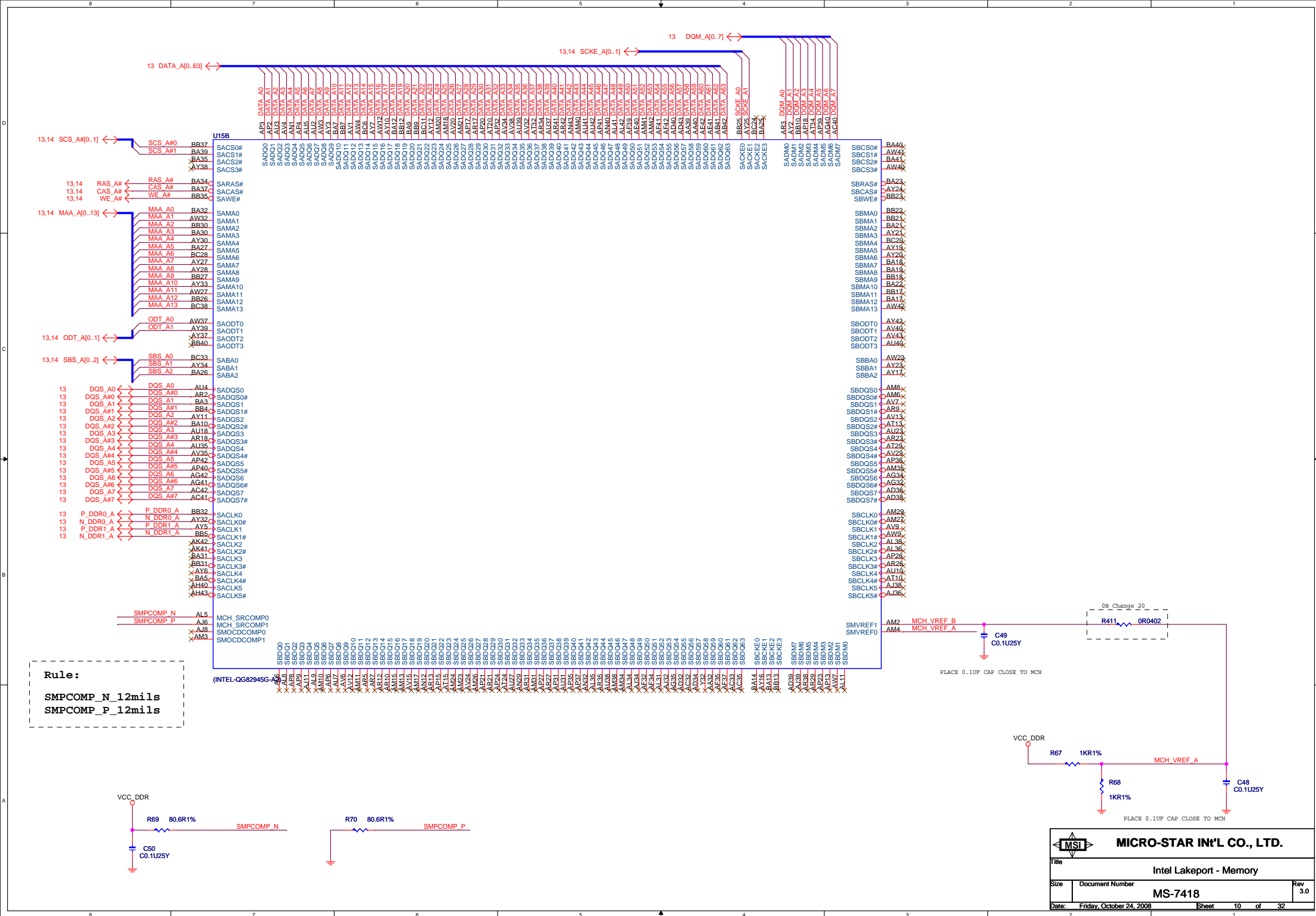
JBAT1	(1-2)NORMAL	(2-3)CLEAR
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CPU SIGNAL BLOCK

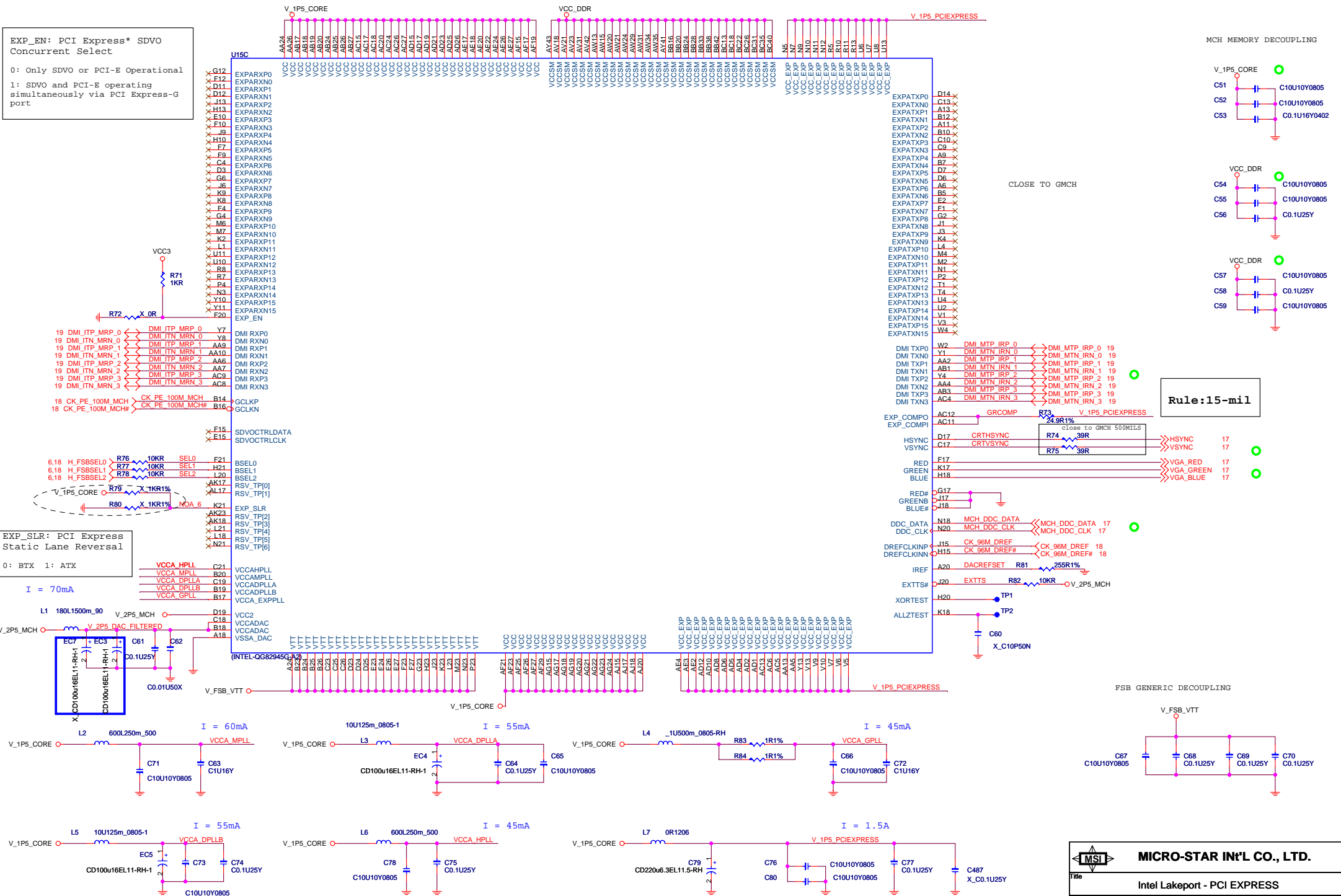


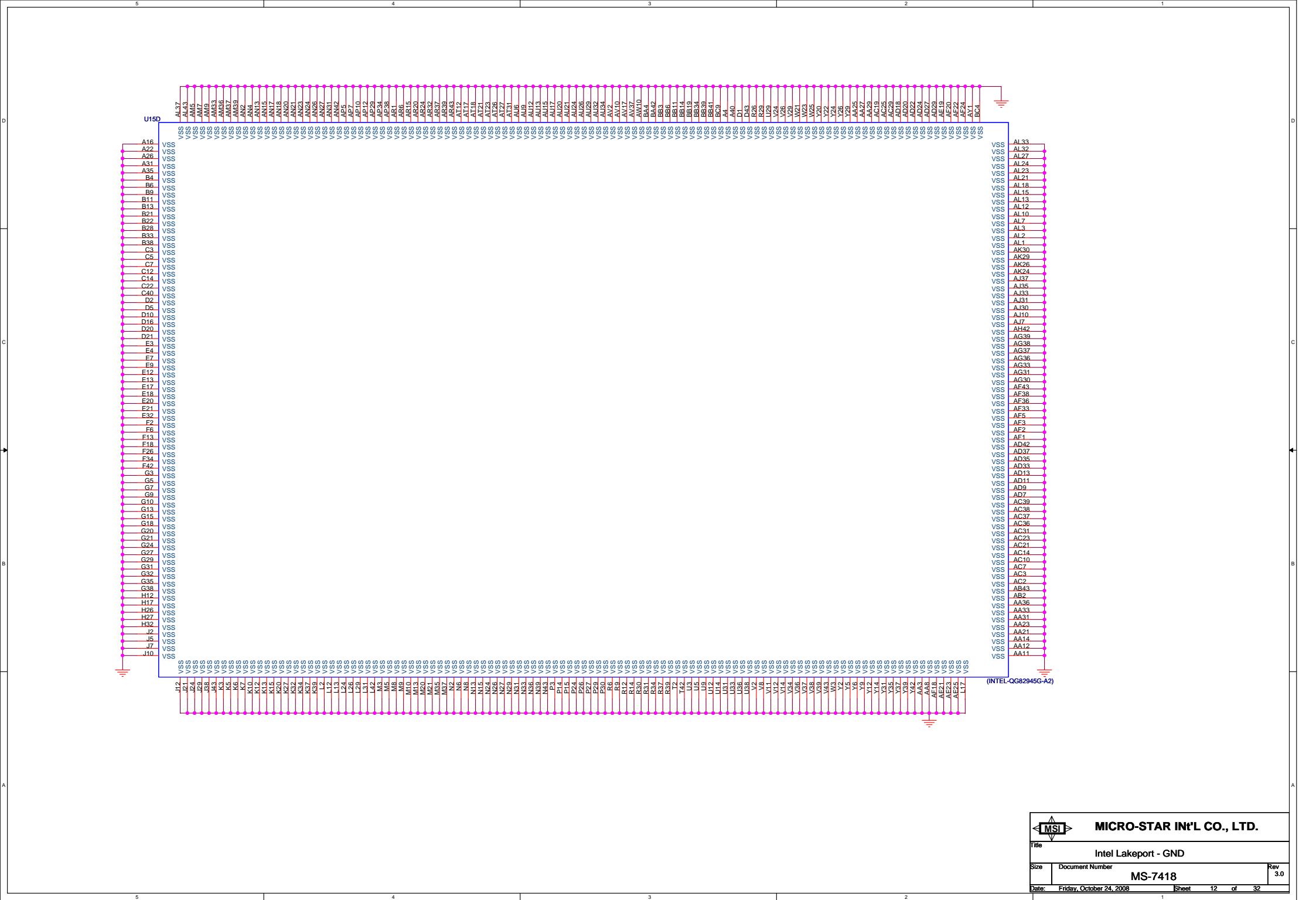




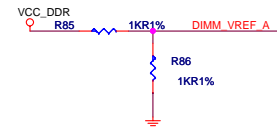
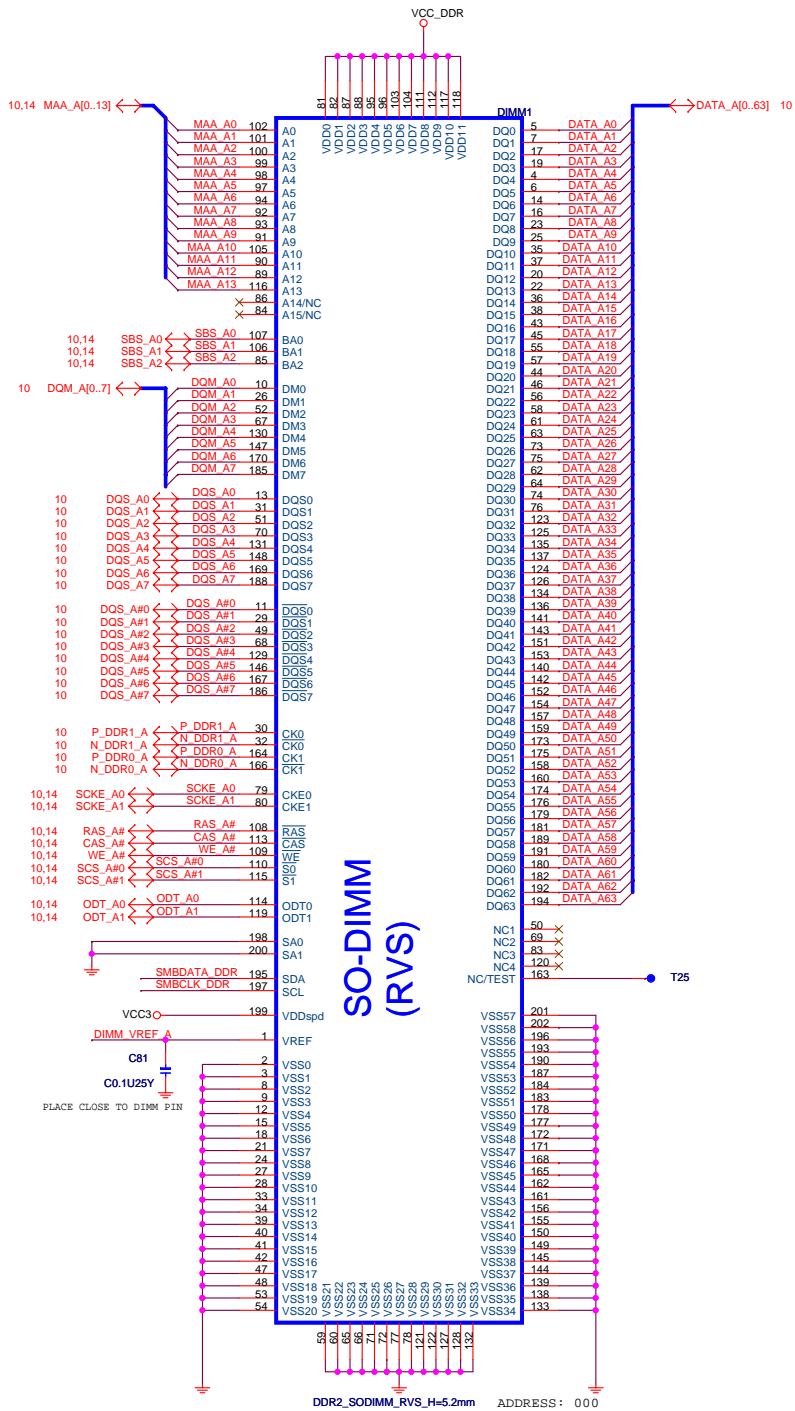


```
0: Only SDVO or PCI-E Operational
1: SDVO and PCI-E operating
simultaneously via PCI Express-G
port
```





DDR2 SO-DIMM



MICRO-STAR INT'L CO., LTD.

DDR II SO-DIMM

Size **MSB** Document Number

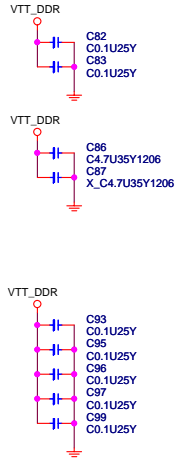
MS-7418

Rev
3.0

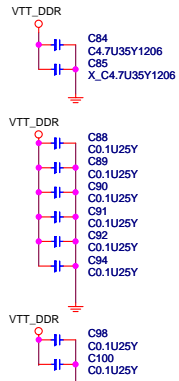
Date: Friday, October 24, 2008

Sheet 13 of 32

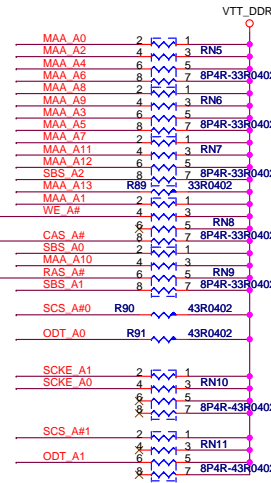
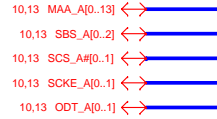
CHANNEL A V_SM_VTT
DECOULPING CAPS



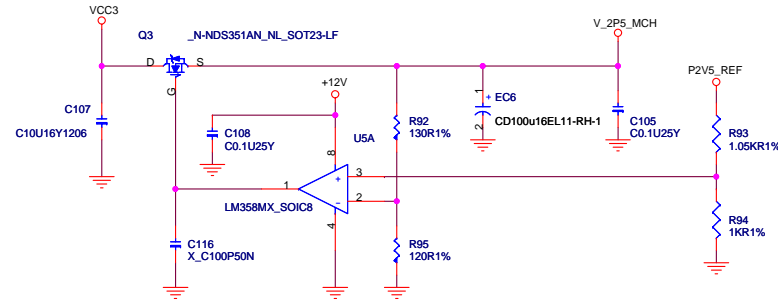
CHANNEL B V_SM_VTT
DECOULPING CAPS

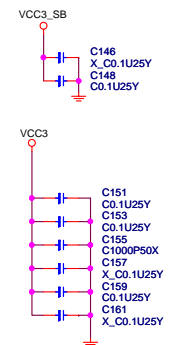
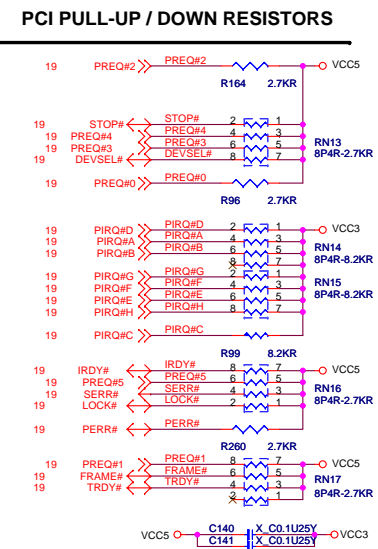


SCS_A#0 change 43 ohm

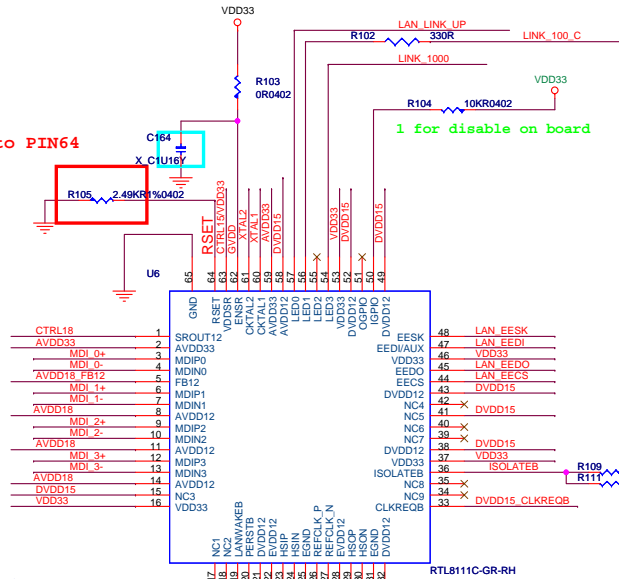


Grantsdale GMCH Power Sequencing
Requirement Between 1.5V Core and 2.5V DAC





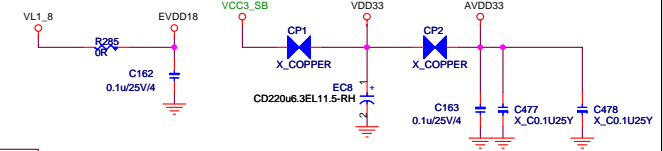
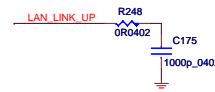
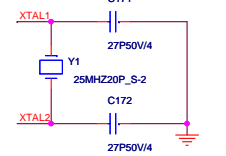
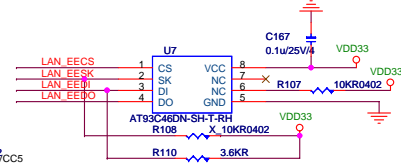
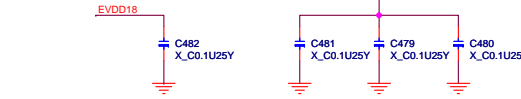
layout close to PIN64



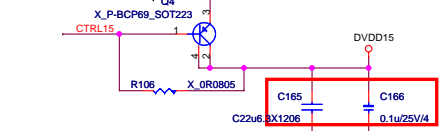
Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

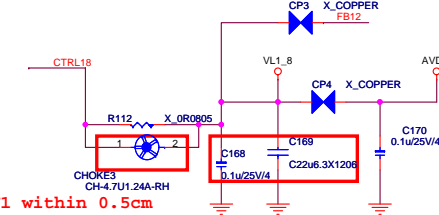
	Q9	Q10
RTL8111B	Need	Need
RTL8111C	N/A	N/A



for 8111B

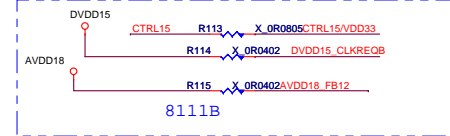


layout close to Q9

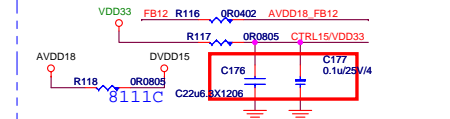


close to PIN1 within 0.5cm

close to choke3 within 0.5cm








close to PIN63 within 0.5cm

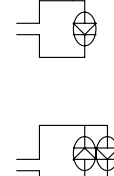
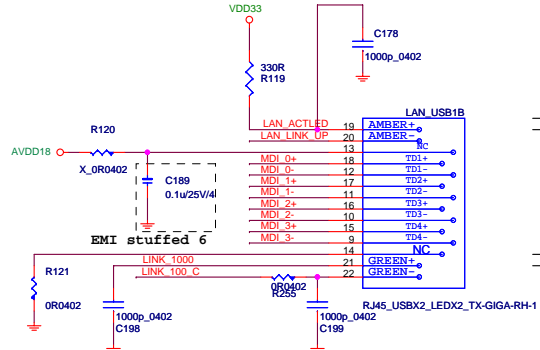
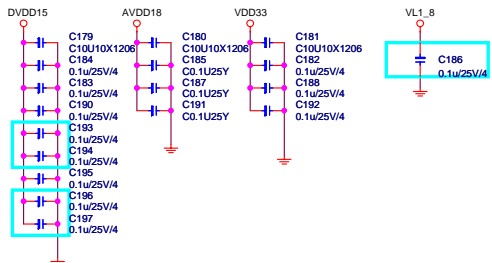


Power consumption		
	1G	100M
3.3V	103mA	TBD
1.5V	367mA	TBD
1.8V	198mA	TBD

-16F0031-F02

Giga-Lan		10/100-Lan	
N58-22F0181-s42		N58-22F0061-s42 N58-22F0061-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	 	21	
22	Green	22	Green

N58-16F0031-F02



Video Connector

Power 20 mils

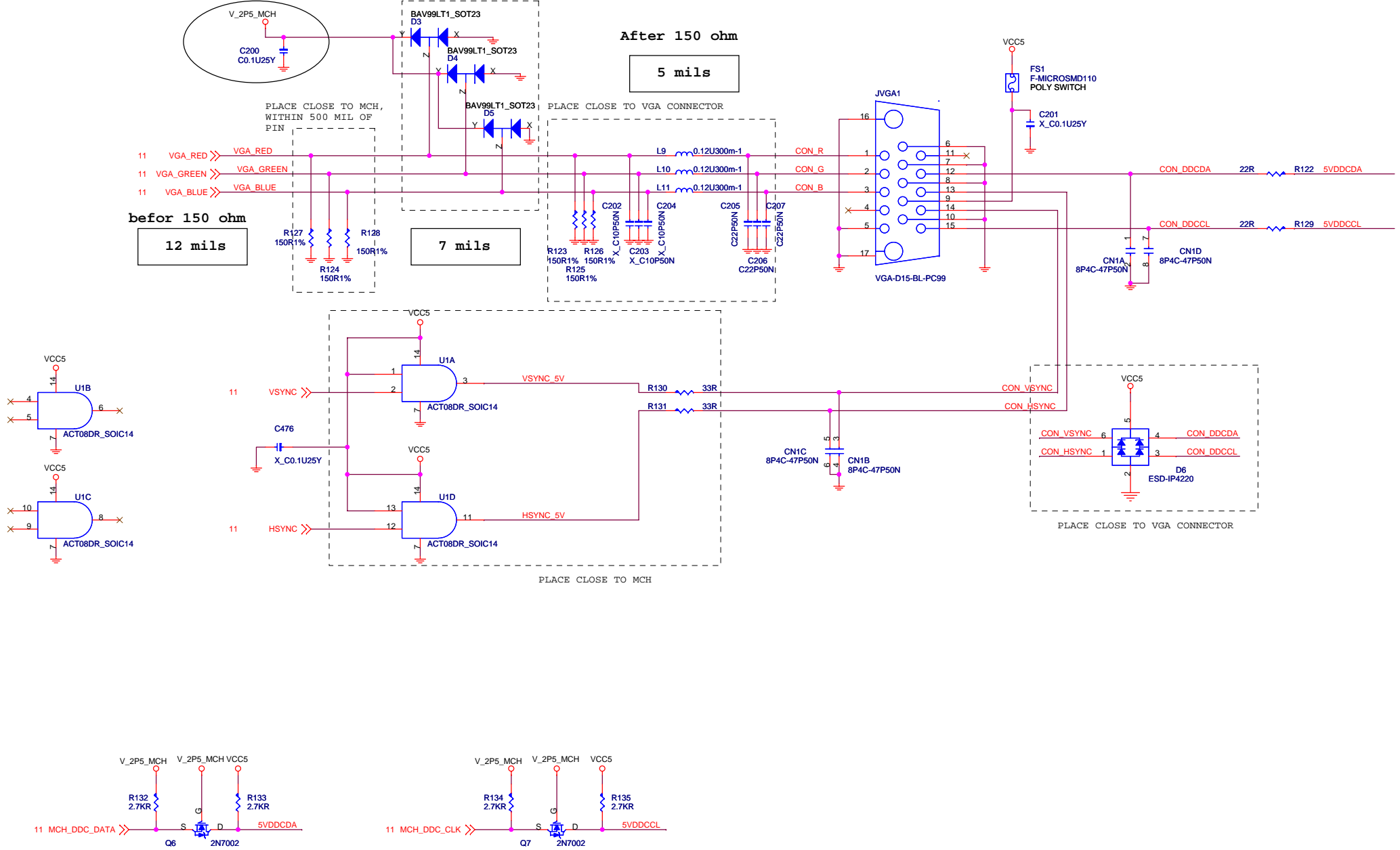
After 150 ohm

5 mils

before 150 ohm

12 mils

7 mils



Trace length less than 0.5inches

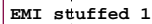
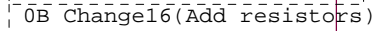
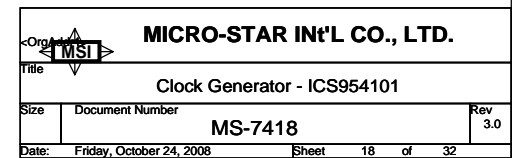
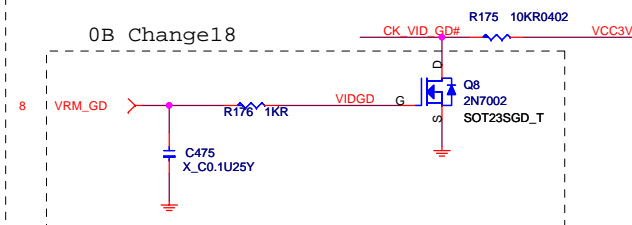
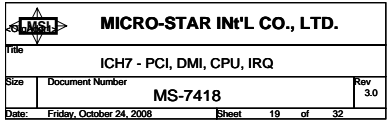


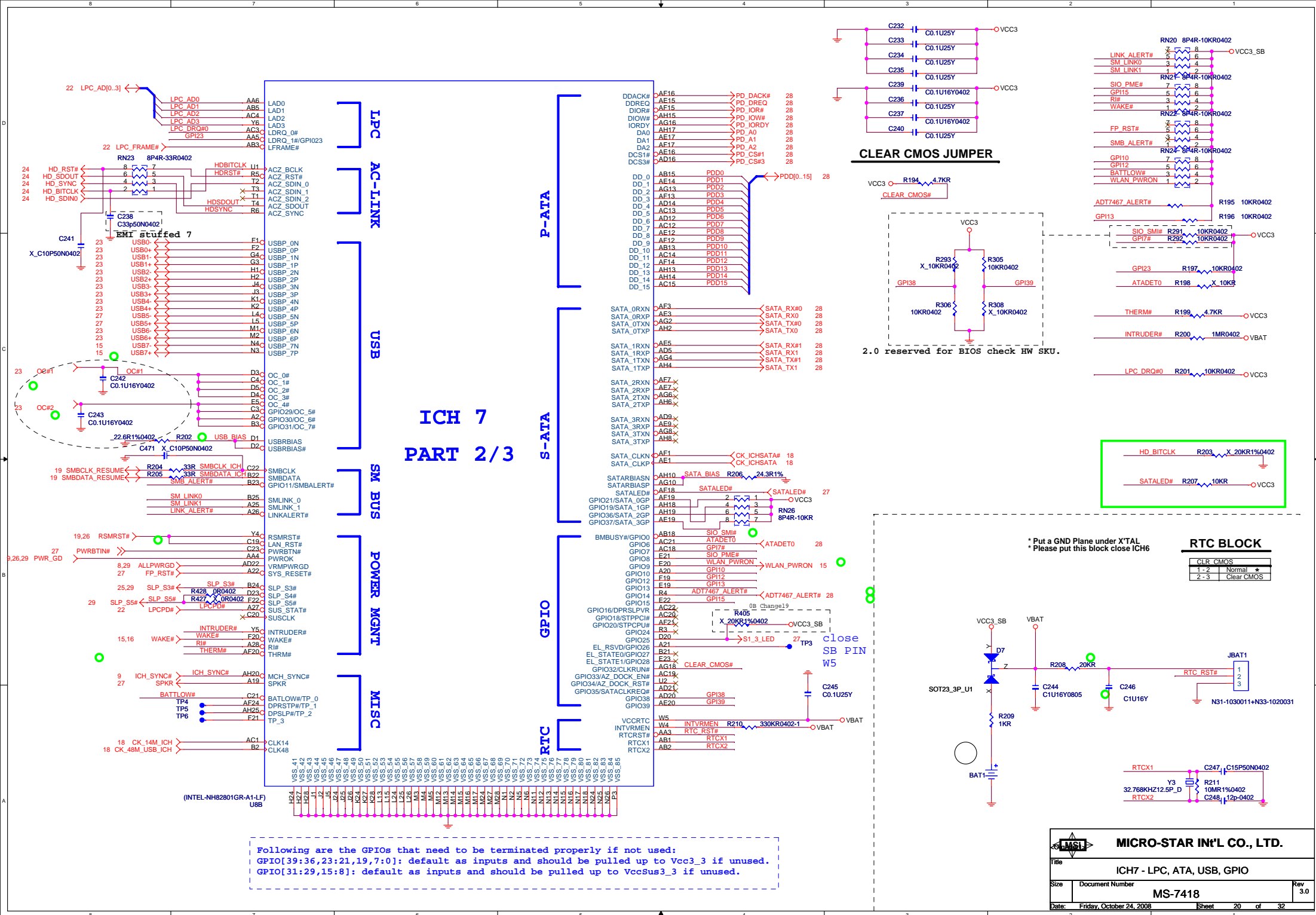
Diagram illustrating the pinout for the 8P4R-1KR0402 connector, showing connections for FSB, FSA, and FSC signals.

Signal	Pin	Label
FSB	8	7, 8
FSA	6	5, 6
FSC	2	1, 2

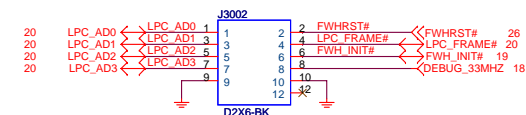
Additional labels: 6, 11, H_FSBSEL1; 6, 11, H_FSBSEL0; 6, 11, H_FSBSEL2; RN18; 8P4R-1KR0402.



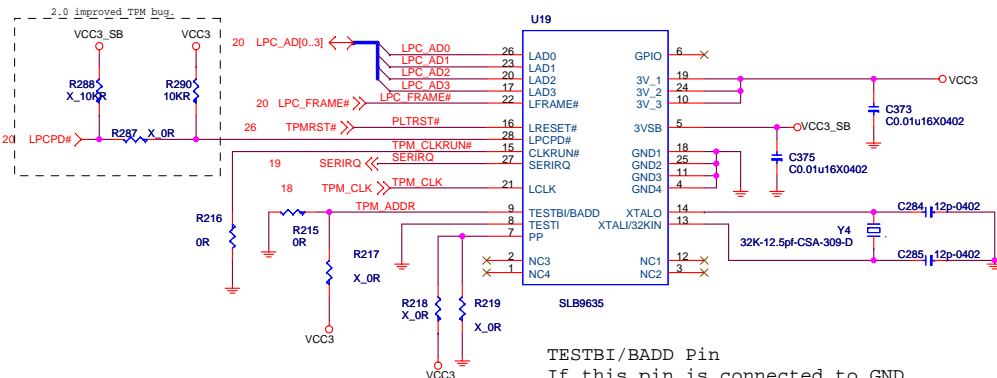




LPC Debug Port

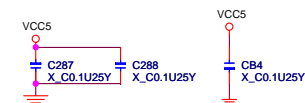
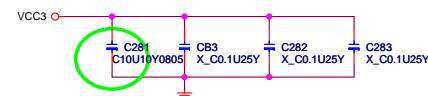


IO Address: 0x02E



TESTBI/BADD Pin

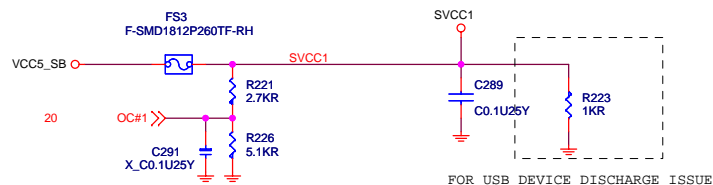
If this pin is connected to GND,
addresses 2EH/2FH are used.
If it is strapped to VCC,
addresses 4EH/4FH are used.



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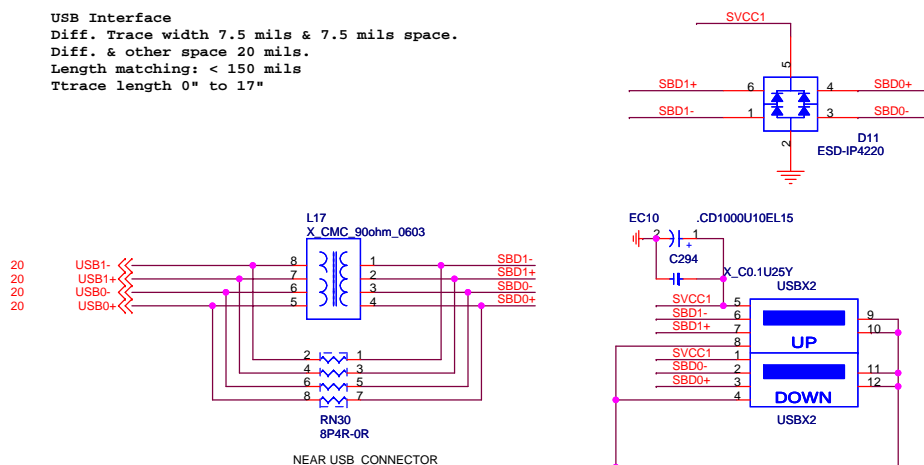
Title			
FWH			
Size	Document Number		Rev
	MS-7418		3.0
Date:	Friday, October 24, 2008		Sheet 22 of 32

POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)



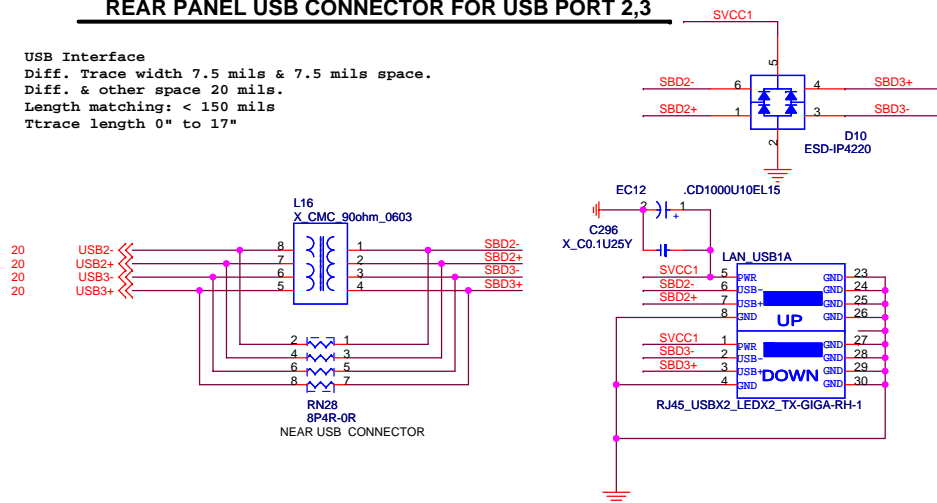
REAR PANEL USB CONNECTOR FOR USB PORT 0,1

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"

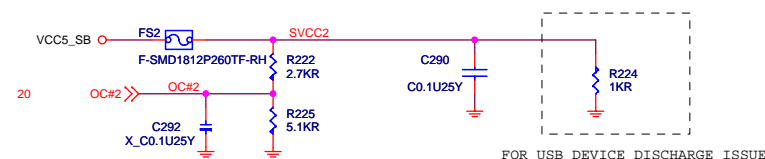


REAR PANEL USB CONNECTOR FOR USB PORT 2,3

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"

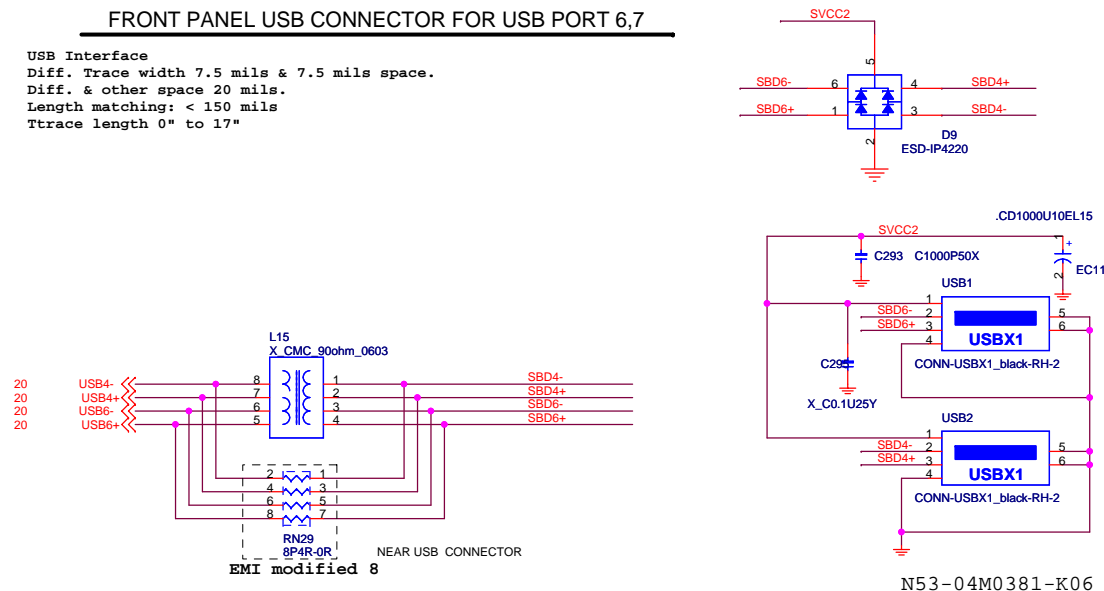


POWER CIRCUIT FOR USB PORT 4,6,7 (FRONT)



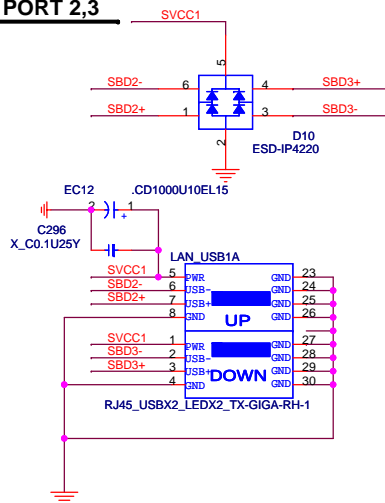
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"

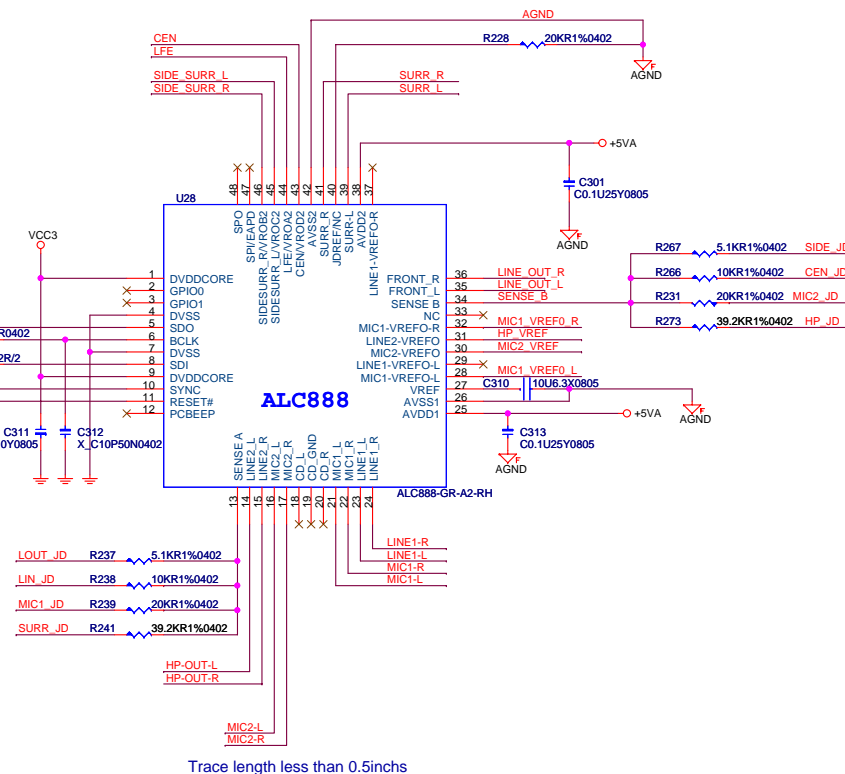


FRONT PANEL USB CONNECTOR FOR USB PORT 4

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"

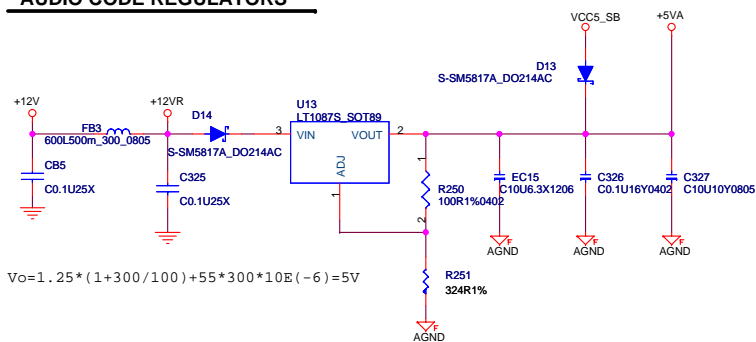


ALC888



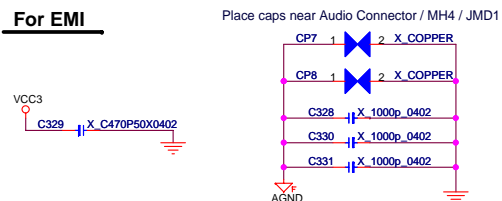
Trace length less than 0.5inches

AUDIO CODE REGULATORS

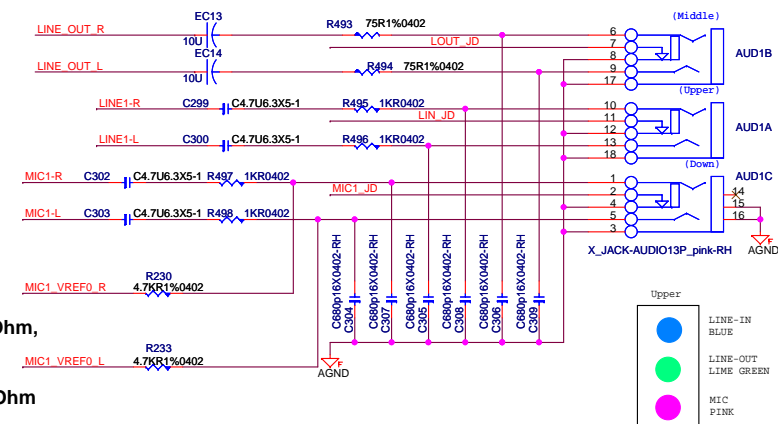


$$V_O = 1.25 * (1 + 300/100) + 55 * 300 * 10E(-6) = 5V$$

For EMI

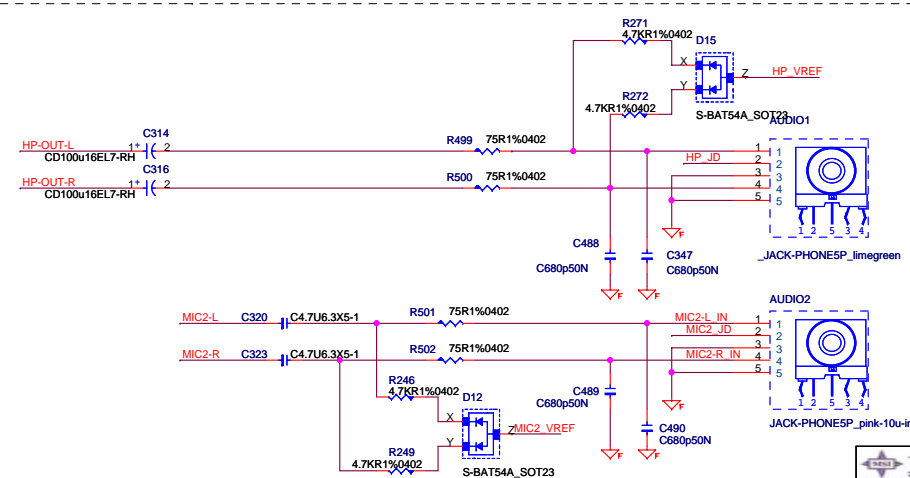
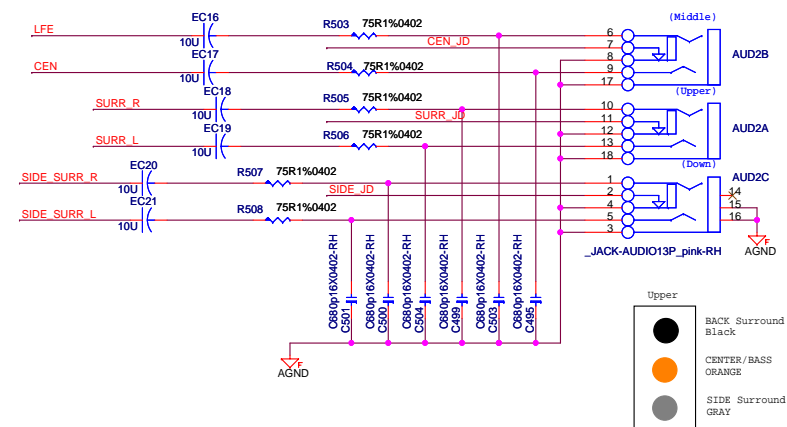


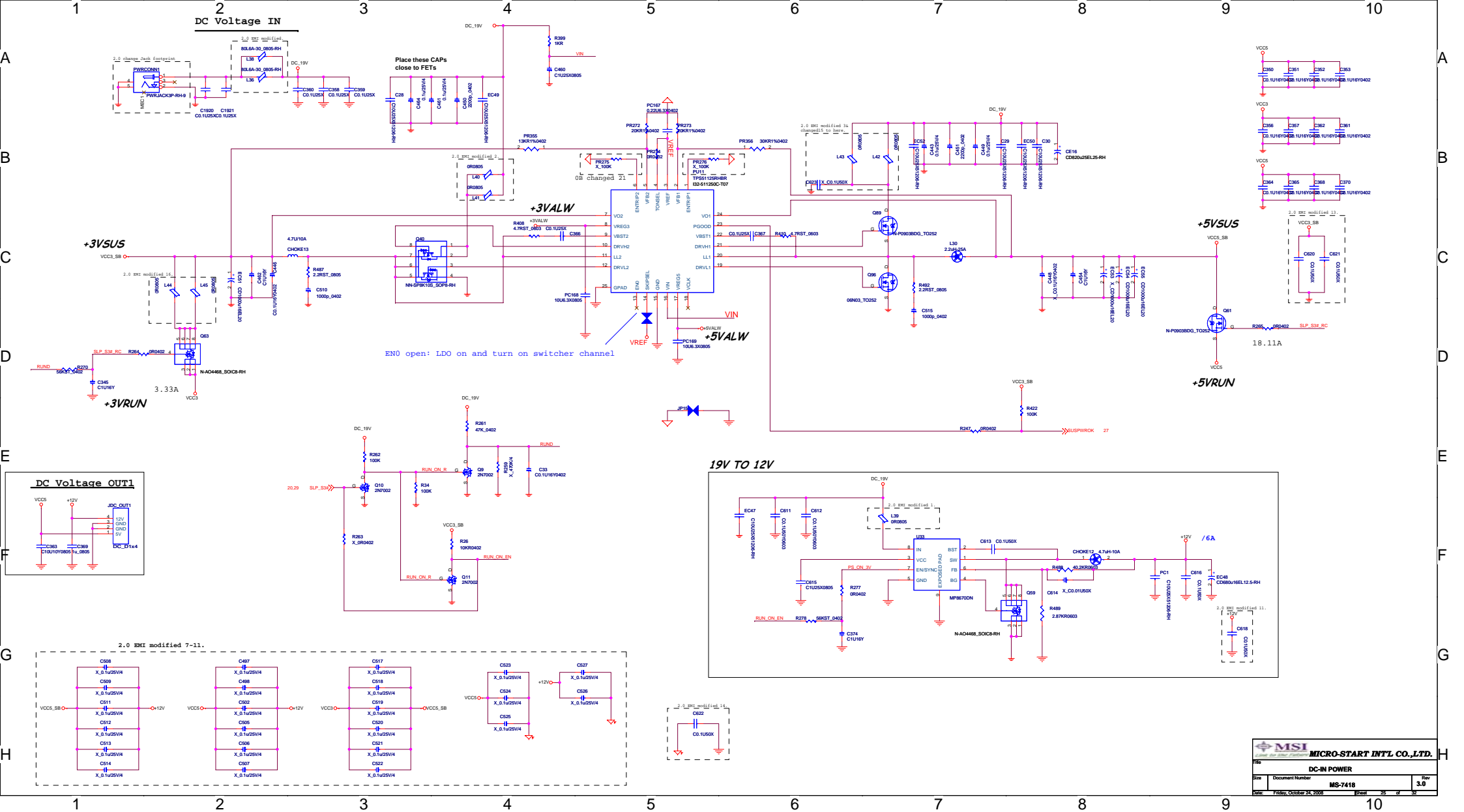
PHONE JACKER (HDA JACK)

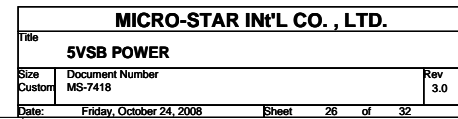
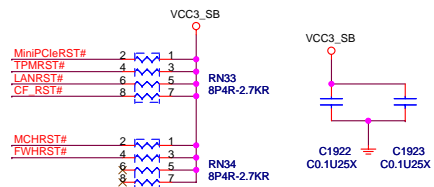


5.1 ch-->N54-13F0171-S42
R495&R496&R497&R498 =75 Ohm,

7.1 ch-->N54-26F0111-K06
R495&R496&R497&R498 =1K Ohm

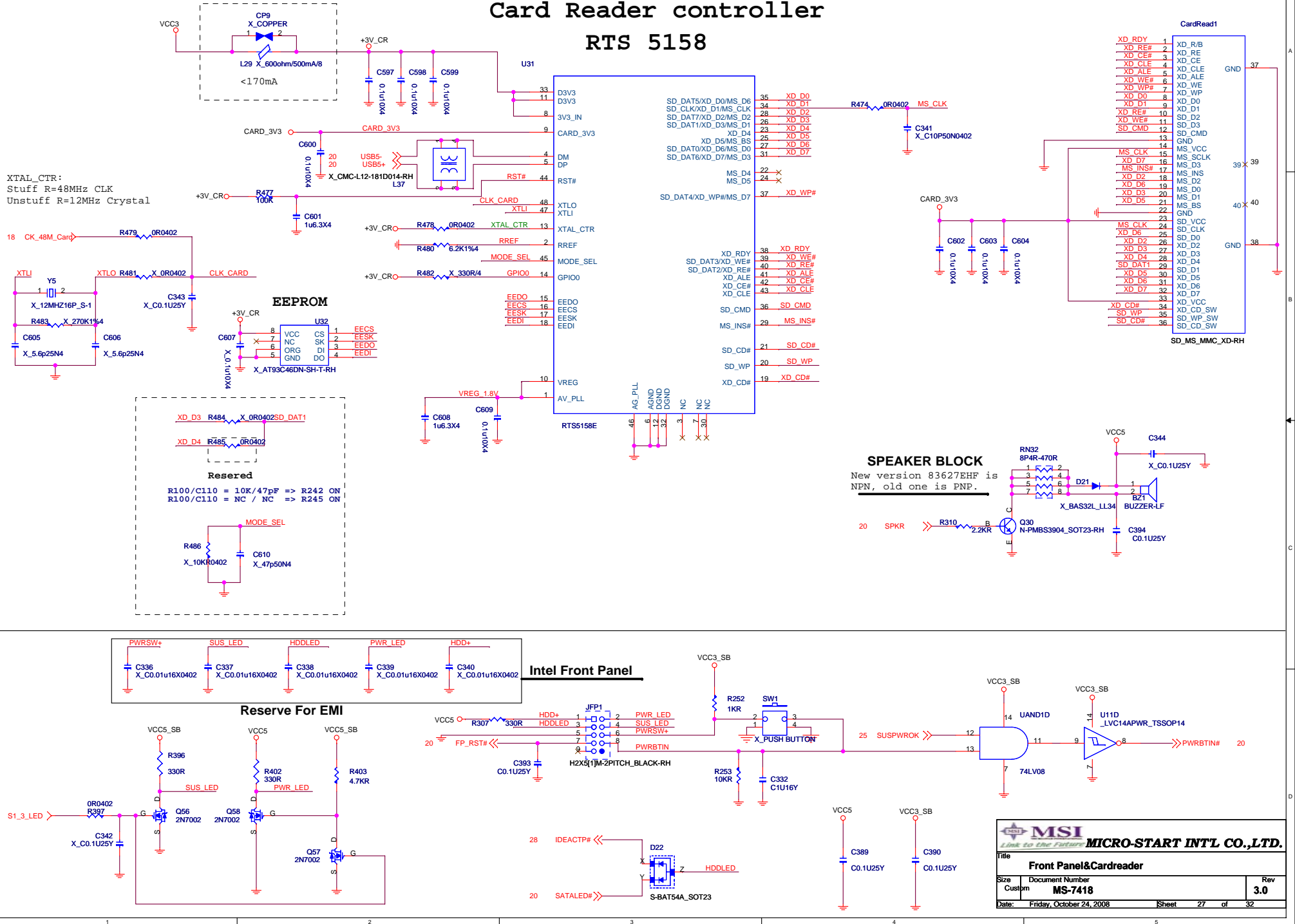




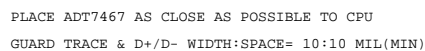
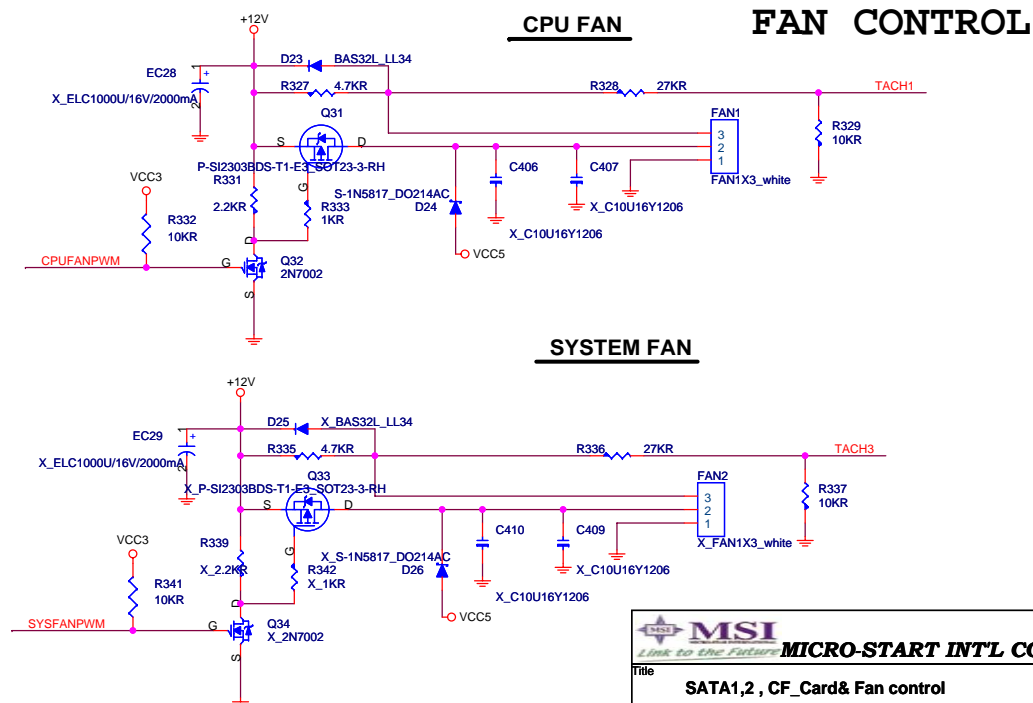
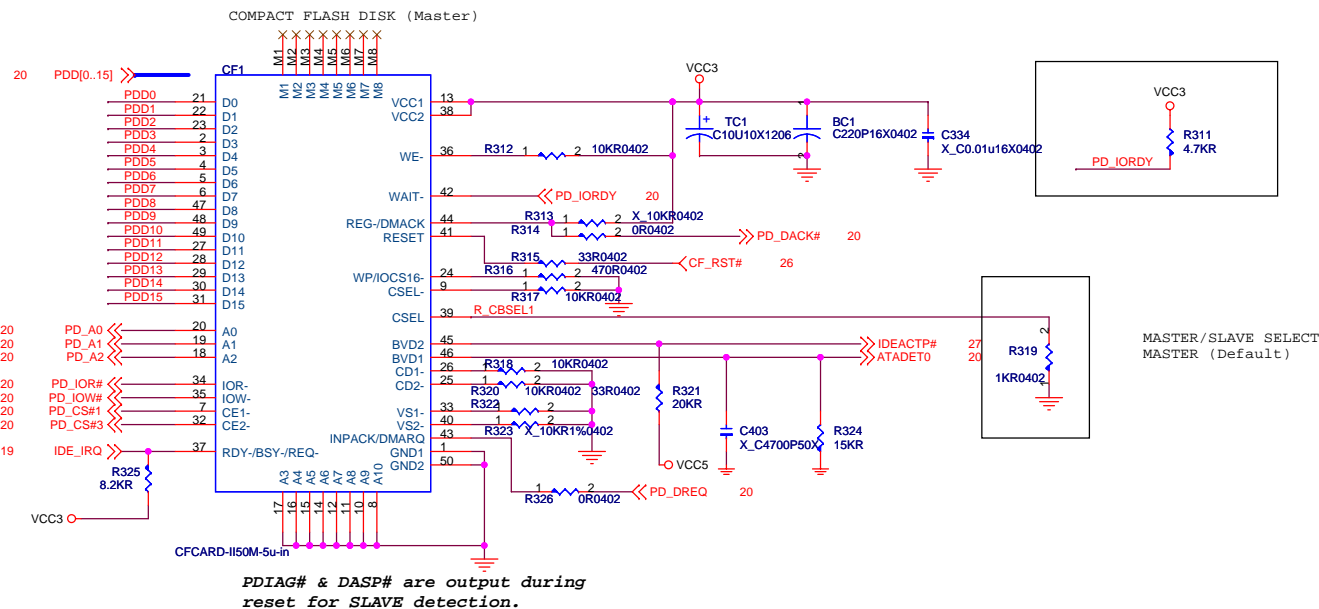


Flash Card Socket

Card Reader controller RTS 5158



COMPACT FLASH CONNECTOR



ACPI Controller

DDR2 1.8V POWER...7.95A

Internal reference $V_{fb}=0.6V$ (+/- 1.5%)
Better than external reference (+/-5%)
==>Using Stand-alone mode

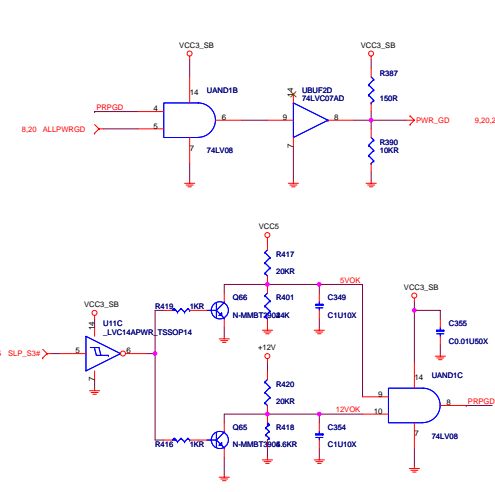
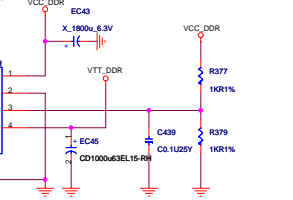
$$V_{fb}=V_{output}*[1.5/(1.5+3.01)]=0.6V \quad V_{output}=1.804V$$

DDR2 1.5V POWER...22.84A

$$V_{fb}=V_{output}*[2/(2+3.01)]=0.6V \quad V_{output}=1.503V$$

VTT1.1V POWER...4.9A

DDR VTT Power

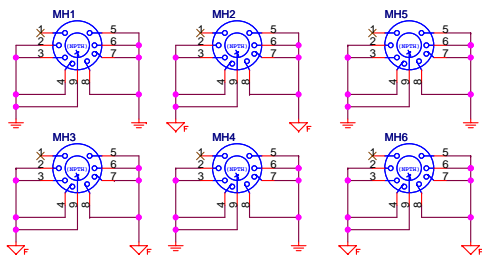


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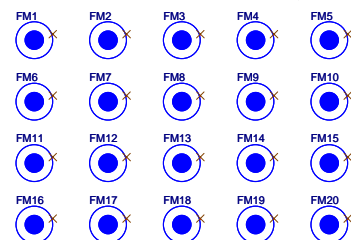
File	MS7 ACPI CONTROLLER	Rev
Size	Document Number	MS-7418
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Auto-BOM Manual Parts

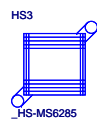
Mounting Holes



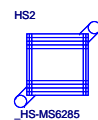
Optics Orientation Holes



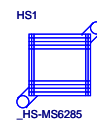
CPU HEAT SINK



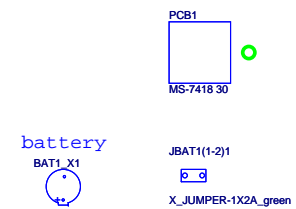
NB HEAT SINK



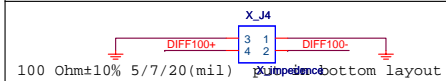
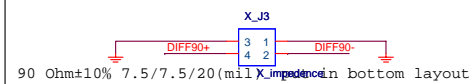
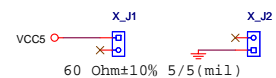
SB HEAT SINK



MANUAL PART



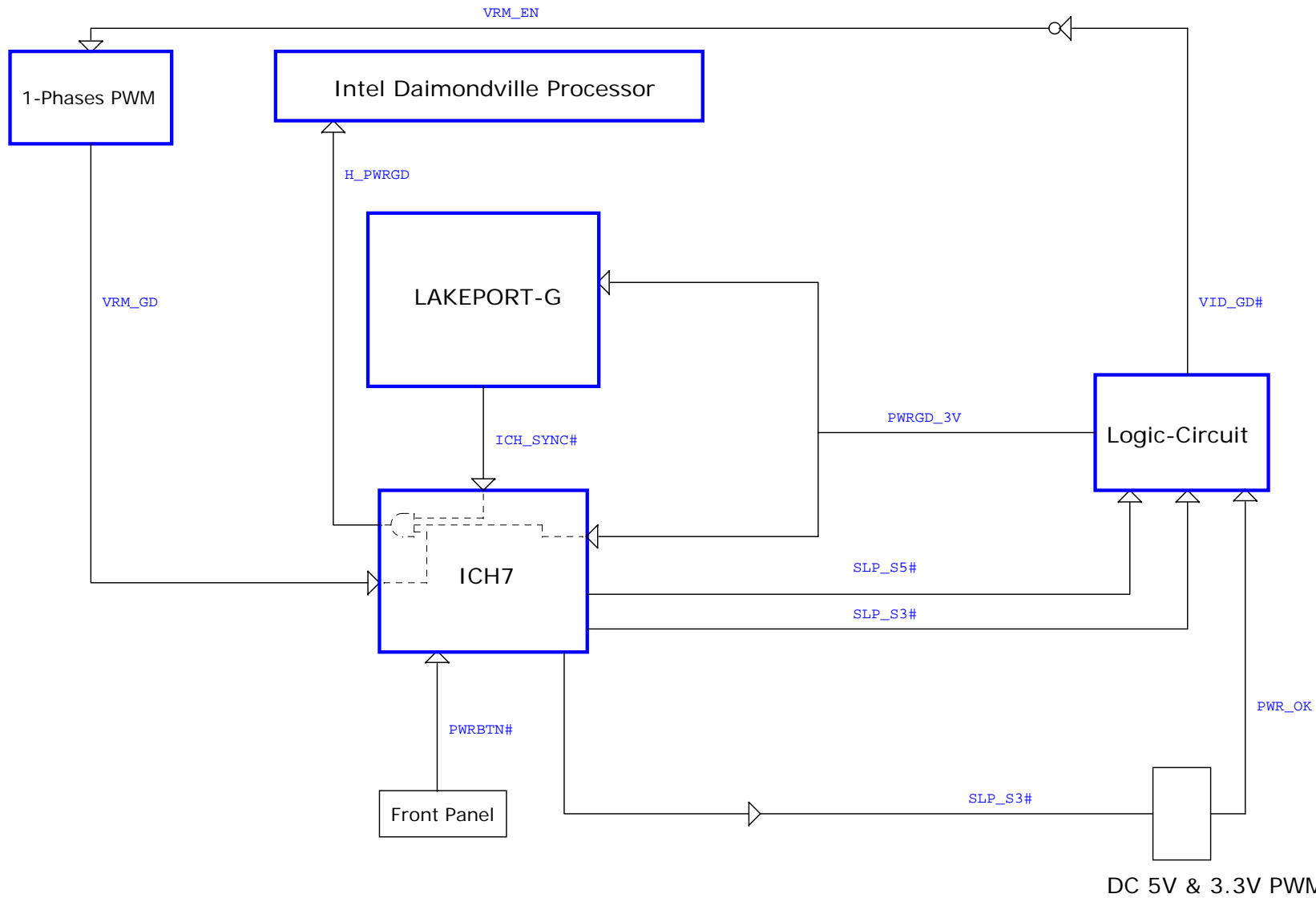
Simulation





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PWROK MAP



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Add ATOM Dual Core circuit.please refer to page 6,7 and 11 that high light in 

CPU Pin M15 Pin name change to TDI_M
CPU Pin L16 Pin name change to TDO_M
CPU Pin G4 Pin name change to THRMDA_2
CPU Pin F4 Pin name change to THRMDC_2
Add R415 to connect PROCHOT and FORCEPR#.
CPU PIN L15, P5, T5, A19
remove C41,C42
Changed pin name and connection to reserved
Add H_COMPX_2,H_GTLREF_2,H_BPM_2.
Change 1.8V enable signal from S5 to S4.
swap BMP signals.
H_BPM#1 to RN35.7
H_BPM#0 to RN35.5
H_BPM#2 to RN35.3
H_BPM#3 to RN35.1
Remove C41,C42 for EMI spacing.
Change CPU to DualCore part number A09-16200D5-I06.

Change L39~L45 from bead to 0 ohm for waveform overshoot issue.
Change Q89 to D03-0480900-O05 and Q96 to D03-0480600-O05.
Change SO-DIMM and CF CARD.

Change R40 from 14.7k to 12k.
Change R45 from 487R to 1.2k.
Add R56 by 3k and unstuff R55.
change R30 from 100k to 20k and C13 from 0.1u to 10u.
change UBUF1,UBUF2 vendor from T07 to P03.
change CPU&NB heatsink part number.
change CPU part number.